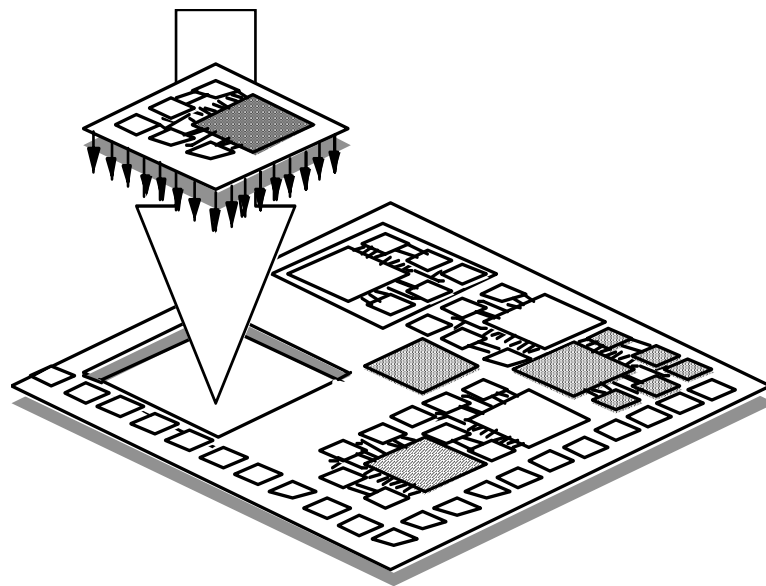


VSI Alliance™
Deliverables Document
Version 2.6.0
(DD 2.6.0)

April 2002



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Revision History

Revision Number	Date	Changes made by	Description of Changes
0.9.0	14Mar98	Larry Saunders	Created initial document from existing VSIA Architecture Document and other information.
1.9.0	18Jul98	Larry Cooke	Updated to include OCB and I/V Specifications and other edits.
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2.0	31Aug99	Editing Staff	Edited formats.
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2.3	17Oct00	Larry Cooke, Stan Baker, Editing Staff	Formatted to match current VSIA styles. Updated tables according to recent Audits of Specifications.
2.4.0	14Dec00	Editing Staff	Edited formats. Updated table formats.
2.4.1	26Feb01	Editing Staff	Corrected error in Table 1, Analog/Mixed-Signal section. Moved Comment in row Section 2.6.6 to Comment cell in row Section 2.6.7.
2.5.0	06Jan01	Editing Staff	Updated OCB 1 2.0 pages of Table 3, page 2, glossary, deleted Appendix E
2.6.0	02Apr02	Editing Staff	Include information from AMS 2 1.0
2.6.0	02May02	Editing Staff	Update Summary and Definition of Terms

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1. Specification Philosophy

The Virtual Socket Interface Alliance (VSIA) specifications identify information required to enable Virtual Components (VCs) integration onto a System on a Chip (SoC). While some of this information comes in the form of documentation, much of it comes as executable models or machine-readable design descriptions.

- The goal of the VSIA is to specify a complete interface that: Provides a practical, reliable link between the VC provider and the VC integrator.
- Evolves consistently with tool, process, and technological advances.
- Specifies the use of an industry standard open format whenever applicable for executable or machine-readable models.

The VSIA advocates convergence among competing formats to reduce the number of recommended alternatives where no standard exists, or where the standard has not yet been widely integrated, the VSIA will encourage standards to be developed by the appropriate associations such as OVI, IEEE, and so forth. The VSIA will endorse standards that meet their requirements.

The VSIA will recommend a proprietary format in a specification only if the owner of the format agrees to make the format available for use within the field of use as defined in the VSIA specification as an open format or for a non-discriminatory and non-burdensome fee.

2. Deliverables Summary

The following summarizes the VSIA Requirements for data formats. The discussion in this section is also applicable to tables in Section 2 of each of the DWG Specification documents. The following list describes the columns in the tables and the keywords used in the columns.

DWG Spec	<p>Specifies the DWG Specification document that contains the deliverable, the format is: [DWG_name] [Spec #] [Major_ver #] . [Minor_ver #] where DWG_name is one of the following:</p> <table border="0"> <tr><td>VCT</td><td>VC Transfer</td></tr> <tr><td>SLD</td><td>System Level Design</td></tr> <tr><td>TST</td><td>Manufacturing Related Test</td></tr> <tr><td>IPP</td><td>IP Protection</td></tr> <tr><td>OCB</td><td>On Chip Busses</td></tr> <tr><td>AMS</td><td>Analog/Mixed-Signal</td></tr> <tr><td>I/V</td><td>Implementation/Verification</td></tr> <tr><td>VER</td><td>Functional Verification</td></tr> <tr><td>QTY</td><td>VC Quality</td></tr> </table> <p>Spec # is a digit from 0 to 9 Major_ver # is a digit from 0 to 9 Minor_ver # is a digit from 0 to 9</p> <p>Note: Any reference to Arch 1.0 denotes that the deliverables are specified in the corresponding section of the Architecture Document 1.0.</p>	VCT	VC Transfer	SLD	System Level Design	TST	Manufacturing Related Test	IPP	IP Protection	OCB	On Chip Busses	AMS	Analog/Mixed-Signal	I/V	Implementation/Verification	VER	Functional Verification	QTY	VC Quality
VCT	VC Transfer																		
SLD	System Level Design																		
TST	Manufacturing Related Test																		
IPP	IP Protection																		
OCB	On Chip Busses																		
AMS	Analog/Mixed-Signal																		
I/V	Implementation/Verification																		
VER	Functional Verification																		
QTY	VC Quality																		
Section	References the document section that discusses the deliverable.																		
Deliverable	Describes the deliverable.																		
VSIA Endorsed Formats	Lists the formats being developed as standards, which meet the VSIA DWGs requirements.																		
Document	Information exchanged on paper or electronically in a widely used format.																		
ASCII	Information must be exchanged in a machine- and human-readable format.																		
VSIA Specified Formats	Lists currently available open formats that have been approved by the respective VSIA DWG.																		
TBD	Denotes that no candidate has been selected. The VSIA will either: - Actively pursue a candidate within a DWG- Will not pursue a candidate at this time																		
Soft, Firm, Hard, AMS Hard, SI Hard	Describes the applicability of the deliverable to a VC of this hardness.																		
OCBD, VCD, SOCI	Describes the applicability of the deliverable to an On-Chip Bus provider, VC Developer, and a System on Chip integrator.																		
M	Denotes Mandatory. Mandatory is a deliverable that is required to make most chip designs workable that use the particular “hardness” of VC denoted by the column it resides in.																		
CM	Denotes Conditionally Mandatory (requirement is based on application).																		

R	Denotes Recommended. Recommended is a deliverable that will improve the design time, quality, or accuracy for most chip designs that use the particular “hardness” of VC denoted by the column it resides in.
CR	Denotes Conditionally Recommended (requirement is based on application). Conditional comments should identify a class of designs, VCs, or chips containing VCs, where this deliverable is applicable if the defined condition is met. Conditions are sufficiently described to delineate the class of designs.
-	This deliverable is not applicable for this category
Comply?	This column is used only by VC providers to indicate compliance with sections of specifications. (See Appendix D)
Comments	Adds clarifying information. The specific conditions necessary to meet a CM or a CR are described within the comments section for each deliverable. Also used by VC providers for comments or references to comments in the comment section of a compliance report. (See Appendix D)

Note: With respect to compliance, all lists of formats for a given category and deliverable, may be viewed as OR of the individual formats. That is, any of the listed formats may be used to satisfy the deliverable.

Table 1: VSI Alliance Specification (AMS 1 2.2) Data Deliverables

Section	Deliverable	VSI Endorsed Formats	VSI Specified Format(s)	A/MS Hard	Comply ?	Comments
2.1	User Guide					
2.1.1	Specification					
2.1.1.1	System Description		document	M		
2.1.1.2	Block Diagram		document	M		
2.1.1.3	Register Description		document	CM		If there are registers present, this deliverable is M.
2.1.1.4	Timing Diagram		document	M, R		If there is digital I/O, this deliverable is M. If there is analog I/O, this deliverable is R.
2.1.1.5	Clock Distribution		document	CM		If there is a clock, this deliverable is M.
2.1.1.6	Bus Interfaces & I/O Configs		document	M		
2.1.1.7	Test Description Summary		document	M		
2.1.1.8	Integration Requirements		document	R		
2.1.1.9	Schematic Block Diagrams		document	R		
2.1.1.10	Operating Modes		document	M		
2.1.1.11	Bias Supply Management		document	CM		If there is a bias supply, this deliverable is M.
2.1.1.12	Operating ranges		document	M		
2.1.1.13	Power Supplies		document	M		
2.1.1.14	Electrical Specifications		document	M		
2.1.1.15	Bonding Pad Requirements		document	CM		If special pads are required, this deliverable is M.

Table 1: VSI Alliance Specification (AMS 1 2.2) Data Deliverables (Continued)

Section	Deliverable	VSI Endorsed Formats	VSI Specified Format(s)	A/MS Hard	Comply ?	Comments
2.1.2	Claims and Assumptions		document	M		
2.1.3	Verification of Claims		document	M		
2.1.4	Version History		document	M		
2.1.5	Known Bugs		document	M		
2.1.6	Application Notes		document	R		
2.2	Process Definition					
2.2.1	Process Requirements		document	M		
2.2.2	Process Tolerances		document	M		
2.2.3	Process Sensitivities		document	R		
2.2.4	Process Design Rule Exceptions		document	CM		If the design rules are intentionally violated, this deliverable is M.
2.2.5	VC Processing History/ Portability		document	R		
2.3	System Architecture and Design					
2.3.1	Algorithmic Level Model		TBD- electronic format pertaining to the tool	R		VSIA may define a more specific format or set of formats at a later time.
2.3.2	System Evaluation Model / Behavioral Model		TBD- electronic format pertaining to the tool	R		VSIA may define a more specific format or set of formats at a later time.
2.3.3	Bonded Out VC/ Prototype		Packaged Integrated Circuit, document	R		

Table 1: VSI Alliance Specification (AMS 1 2.2) Data Deliverables (Continued)

Section	Deliverable	VSI Endorsed Formats	VSI Specified Format(s)	A/MS Hard	Comply ?	Comments
2.4	Functional and Performance Modeling					
2.4.1	Digital Placeholder (“Dummy”) Model		Verilog, VHDL	R		
2.4.2	Functional/ Timing Digital Simulation Model		Verilog, VHDL	R		
2.4.3	Digital Timing Model for Static Timing	OLA		R		
2.4.4	Bus Functional Model (for digital interfaces)		TBD	R		Format to be determined by the VSI SLD Interface subgroup.
2.4.5	Peripheral Interconnect Model (for digital interfaces)		SPEF	CM		If there is a measurable level of interconnect between the I/O ports and the internal gates of the VC, this deliverable is M.
2.4.6	Electrical Port Models					
2.4.6.1	Digital Electrical Port Model (device level interface netlist)		VC Hspice	R		
2.4.6.2	Analog Electrical Port Model		VC Hspice	R		
2.4.7	Block level HDL Simulation Model	Verilog-AMS, VHDL-AMS		R		

Table 1: VSI Alliance Specification (AMS 1 2.2) Data Deliverables (Continued)

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Format(s)	A/MS Hard	Comply ?	Comments
2.4.8	Detailed Transistor/Gate Level Schematics		any suitable format	CR		If the VC provider agrees to release this deliverable, it is R. There may be IP Protection issues requiring discussion between the VC provider and the VC integrator.
2.4.9	Circuit Level Simulation Netlist		VC Hspice	CR		If the VC provider agrees to release this deliverable, it is R. There may be IP Protection issues requiring discussion between the VC provider and the VC integrator.
2.5	Test Support					
2.5.1	Signal Requirements		document	M		
2.5.2	Test Requirements		document	M		
2.6	Physical Block Implementation					
2.6.1	Detailed Physical Block Description		GDSII-Stream	M		
2.6.1.1	Layer Mapping Table		document	M		
2.6.2	Pin List/Pin Placement		VC LEF	M		
2.6.3	Routing Obstructions		VC LEF	M		
2.6.4	Footprint		VC LEF	M		
2.6.5	Power and Ground		VC LEF	M		
2.6.6	Layer Mapping Table		document	M		

Table 1: VSI Alliance Specification (AMS 1 2.2) Data Deliverables (Continued)

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Format(s)	A/MS Hard	Comply ?	Comments
2.6.7	Physical Netlist		VC Hspice	CM		If layout versus schematic is required by the VC integrator, this deliverable is M.
2.6.8	General Physical Rules					
2.6.8.1	Physical Isolation Specification		document	M		
2.6.9	Placement Specifications					
2.6.9.1	Placement Constraints		document	M		
2.6.9.2	Proximity Effects		document	M		
2.6.10	Interconnect Specifications					
2.6.10.1	Special Hookup Guidelines		document	M		
2.6.10.2	Routing Constraints		document	M		

Table 2: Summary of Deliverables Table (AMS 2 1.0)

Section	Deliverable	Currently Used Formats	VSIA Specified Format	SI Hard	Comply ?	Comments
2.1	Interconnect Crosstalk (Voltage Noise and Delay Variance) and Signal Electromigration					
2.1.1	Overview					
2.1.2	Electrical Data					
2.1.2.1	Maximum Permissible Noise Propagating into Input Ports		VC Hspice	CM		If available, otherwise document in Section 2.4
2.1.2.2	Maximum Permissible Noise Injected into Failure-critical Nets (If Any) Inside VC		VC Hspice	CM		If available, otherwise document in Section 2.4

Table 2: Summary of Deliverables Table (AMS 2 1.0) (Continued)

Section	Deliverable	Currently Used Formats	VSI Specified Format	SI Hard	Comply ?	Comments
2.1.2.3	Maximum Permissible External (to VC) Switching Cross-coupling for Delay-critical Sensitive Nets (If Any) Inside VC		SPEF	CM		If available, otherwise document in Section 2.4
2.1.2.4	Maximum Noise Possible at Output Ports (Due to Propagation and Coupling Inside VC)		VC Hspice	CM		If available, otherwise document in Section 2.4
2.1.2.5	Electrical Characteristics for Strong Potential Aggressors (for OTH Signals) Lying Inside VC					
2.1.2.5.1	I/O Driver Models		VC Hspice	R		
2.1.2.5.2	Interconnect Models		SPEF	R		
2.1.2.6	Electrical Characteristics for Failure- or Delay-critical Sensitive Nets Lying Inside VC		VC Hspice, SPEF	R		
2.1.2.6.1	I/O Driver Models		VC Hspice	R		
2.1.2.6.2	Interconnect Models		SPEF	R		
2.1.2.7	Best- and Worst-case Slew Permissible at Input Ports		Hspice, Document			
2.1.2.7.1	Minimum and Maximum Slew Limits		Document	M		
2.1.2.7.2	Input Environment Models		VC Hspice	M		
2.1.2.8	Best- and Worst-case Slew Available at Output Ports (and Its Variation with Load)					
2.1.2.8.1	Minimum and Maximum Slew Limits		Document	M		
2.1.2.8.2	Driver Models		VC Hspice	M		
2.1.2.9	Maximum Permissible Load and Distributed RC that Can Be Driven by Output Ports		SPEF	M		
2.1.3	Physical Data					
2.1.3.1	Location of Failure- or Delay-critical Sensitive Interconnect Polygons Inside VC		PDEF	R		
2.1.3.2	Location of Strong Potential Aggressors (for OTH Signals) Lying Inside VC		PDEF	M		

Table 2: Summary of Deliverables Table (AMS 2 1.0) (Continued)

Section	Deliverable	Currently Used Formats	VSIA Specified Format	SI Hard	Comply ?	Comments
2.1.3.3	Location of Top-layer and Peripheral Supply and Ground Wires Inside VC		PDEF	M		
2.1.3.4	No-fly Zone or External Shielding Requirements		PDEF	R		
2.1.3.5	Safe Regions for OTH Signals (Possibly Classified by Slew)		PDEF	R		
2.1.4	Timing Data					
2.1.4.1	Variation of Timing Arcs within VC with External Crosstalk		SDF	CM		If available, otherwise document in Section 2.4
2.1.4.2	Transition Windows Available at Output Ports		SDF	M		
2.1.4.3	Transition Windows Assumed at Input Ports		SDF	M		
2.1.4.4	Transition Windows for Strong Potential Aggressors (for OTH Signals) or Failure- or Delay-critical Sensitive Nets Lying Inside VC		SDF	M		
2.1.5	Logical Data					
2.1.5.1	Mutex (One-hot) Relationships Assumed Between Input Signals	Pathmill CFG files	Document	M		
2.1.5.2	Mutex (One-hot) Relationships Available Between Output Signals	Pathmill CFG files	Document	M		
2.1.6	Signal Electromigration					
2.1.6.1	Electrical Data					
2.1.6.1.1	Current Density Limits on Metal and Via Layers		Document	M		
2.1.6.1.2	Maximum Load for Electromigration Limits on Outputs		VC Hspice	M		
2.1.6.1.3	Maximum Slew Rate for Electromigration Limits on Inputs		SDF	R		
2.1.6.1.4	Maximum Switching Factor		VC Hspice	R		
2.1.6.1.5	Drive Strength		Document	M		
2.1.6.1.6	Input Load		Document	M		
2.1.6.2	Physical Data		GDSII	M		
2.2	Supply and Ground Grid Noise and Electromigration					

Table 2: Summary of Deliverables Table (AMS 2 1.0) (Continued)

Section	Deliverable	Currently Used Formats	VSIA Specified Format	SI Hard	Comply ?	Comments
2.2.1	Overview					
2.2.2	Electrical Data Specification					
2.2.2.1	Specification Requirements for Static Power Model		Document	M		
2.2.2.2	Specification Requirements for Dynamic Power Model		Document	R		
2.2.3	Physical Data					
2.2.3.1	External Geometrical Data of the Supply and Ground Nets (Supply and Ground Ports)		VC LEF	M		
2.2.3.2	Internal Geometrical Data of the Supply and Ground Nets		Document	M		
2.2.4	Timing Data					
2.2.4.1	Variation in Timing on Output Pins (Delay and Edge Rates) Due to IR Drop in Power Grid	Synopsys .lib file	Document	M		
2.2.4.2	Variation in Timing on Input Pins (Setup and Hold Time) Due to IR Drop in Power Grid	Synopsys .lib file	Document	R		
2.2.5	Multiple Power Supplies for Analog Blocks, Multi-Vt Circuits, and Pads		Document	M		
2.2.6	Supply and Ground Electromigration Verification		Document	M		
2.3	Substrate Noise and Coupling					
2.3.1	Overview					
2.3.2	Electrical Data					
2.3.2.1	Block-level Impedance Model		VC Hspice	M		
2.3.2.2	Noise Sources for Aggressor Access Ports		VC Hspice	M		
2.3.2.3	Maximum Allowed Noise for Each Victim Access Port		VC Hspice	M		
2.3.3	Physical Data					
2.3.3.1	Regions		Document	M		
2.3.3.2	Substrate Access Ports	Annotated GDSII	Document	M		
2.4	SI Requirements Document		Document	M		

Table 3: VSI Alliance Specification (I/V 1 2.1) Data Deliverables

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Formats	Soft	Firm	Hard	Comply ?	Comments
2.1	Implementation Level Behavioral and Structural Models							
2.1.1	RTL Source		Verilog/ VHDL Synthesis Subset	M	CM	CR		Mandatory (M) for Firm VCs if required for synthesis. Required (R) for Hard VCs if formal verification or functional simulation is met.
2.1.2	Cell Level and Circuit Level Netlist		Verilog, EDIF-netlist, VC Hspice, VHDL	--	CM	CM		Mandatory (M) for Firm VCs if they are described at the gate level. Mandatory (M) for Hard VCs if layout versus schematic checking is required for these VCs.
2.2	Implementation Level Performance Models							
2.2.1	Basic Delay Model	OLA		R	M	M		
2.2.2	Timing Analysis Model	OLA		R	M	M		
2.2.3	Power Model							
2.2.3.1	Black/Gray Box Power Model Requirements	OLA		R	M	M		
2.2.3.2	RTL Source Power Model Requirements		Verilog/ VHDL Synthesis Subset	M	--	--		
2.2.3.3	Cell Level Power Model Requirements		Verilog, EDIF-netlist, VHDL, SPEF	--	CR	CR		Recommended (R) if a more accurate power model is required.

Table 3: VSI Alliance Specification (I/V 1 2.1) Data Deliverables (Continued)

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Formats	Soft	Firm	Hard	Comply ?	Comments
2.2.3.4	Circuit Level Power Model Requirements		VC Hspice	--	--	CR		Recommended (R) if a more accurate power model is required.
2.2.4	Peripheral Interconnect Model		SPEF	--	CR	CM		Recommended (R) for Firm VCs and Mandatory (M) For Hard VCs if the peripheral interconnect needs to be included in the delay calculation.
2.2.5	Circuit Level Interface Model Requirements		VC Hspice	--	CM	CM		Mandatory (M) if the IO or interfaces need to be modeled at the circuit level.
2.3	Physical Modeling							
2.3.1	Detailed Physical Block Description		GDSII	--	CM	M		Mandatory (M) if Firm VCs contain physical data.
2.3.2	Pin List/Pin Placement		VC LEF	--	CM	M		Mandatory (M) if Firm VCs contain physical data.
2.3.3	Routing Obstructions		VC LEF	--	CM	M		Mandatory (M) if Firm VCs contain physical data.
2.3.4	Footprint		VC LEF	--	CM	M		Mandatory (M) if Firm VCs contain physical data.
2.3.5	Power and Ground		VC LEF	--	CR	M		Recommended (R) if Firm VCs contain physical data.
2.3.6	Signature		VC LEF	--	--	M		
2.4	Design Constraints							
2.4.1	Timing Constraint	DC-WG		M	M	--		

Table 3: VSI Alliance Specification (I/V 1 2.1) Data Deliverables (Continued)

Section	Deliverable	VSI Endorsed Formats	VSI Specified Formats	Soft	Firm	Hard	Comply ?	Comments
2.4.2	Clock Con- straints	DC-WG		M	M	CM		Mandatory (M) if the clock sig- nal require- ments need to be provided to the Hard VC.
2.4.3	Logic Archi- tecture Con- straints	DC-WG		M	--	--		
2.4.4	Area Con- straints	DC-WG		R	CM	--		Mandatory (M) if Synthesis or Floorplanning is required.
2.4.5	Physical Im- plementation Constraints	DC-WG		CM	CM	--		Mandatory (M) if Floorplan- ning is re- quired.
2.4.6	Power Con- straints	DC-WG		CM	CM	--		Mandatory (M) if Synthesis or Floorplanning is required.
2.4.7	Test Con- straints	DC-WG		M	M	M		
2.4.8	Environmental / Operating Constraints	DC-WG		M	M	M		

Table 4: VSI Alliance Specification (OCB 1 2.0) Data Deliverables

Section	Deliverable	Currently Used Formats	Candidate VSIA Format	OCBD	VCD	SOCI	Comply ?	Comments
2.1	User Guide							
2.1.1	Version Number	Document	Document	M	M	M		
2.1.2	Revision History	Document	Document	M	M	M		
2.1.3	Document Conventions	Document	Document	M	M	M		
2.1.4	Introduction	Document	Document	M	M	M		
2.1.5	Signal Definition	Document	Document	M	M	M		
2.1.6	Bus Operation	Document	Document	M	M	M		
2.1.7	Configuration Space	Document	Document	CM	CM	CM		If the deliverables exist, this deliverable is M.
2.1.8	Core Isolation	Document	Document	R	CM	M		If the VC developer is producing a hard VC, this deliverable is M.
2.1.9	Glossary	Document	Document	R	R	R		
2.2	Implementation Specification	Document	Document	R	R	R		
2.3	Physical Attributes							
2.3.1	Bus Development Tools	VHDL, Verilog	VHDL, Verilog	R	R	R		
2.3.2	Timing Analysis	Document	ASCII	R	R	R		
2.3.3	Simulation Models	VHDL, Verilog	VHDL, Verilog	R	CM	M		If the VC developer is producing a hard VC, this deliverable is M.
2.3.4	Bus Implementation Tools	Verilog, VHDL, C, C++	Verilog, VHDL, C, C++	R	R	R		
2.3.4.1	Bus Protocol Monitor	Verilog, VHDL, C, C++	Verilog, VHDL, C, C++	CR	R	R		If this deliverable is not available from another source, it is recommended for the On-Chip Bus Provider.

Table 4: VSI Alliance Specification (OCB 1 2.0) Data Deliverables (Continued)

Section	Deliverable	Currently Used Formats	Candidate VSIA Format	OCBD	VCD	SOCI	Comply ?	Comments
2.3.4.2	Bus Performance Monitor	Verilog, VHDL, C, C++	Verilog, VHDL, C, C++	CR	CR	R		If this deliverable is not available from another source, it is Recommended for the On-Chip Bus Provider.
2.3.5	Compliance Test Bench	Verilog, VHDL, C, C++	Verilog, VHDL, C, C++	R	M	--		
2.3.6	Debug Tools			R	R	--		No formats exist for these tools.
2.4	Technical Attributes							
2.4.1	General Bus Attributes	Document	Document	M	M	M		
2.4.2	Un-Cached Transaction Attributes	Document	Document	M	M	M		
2.4.3	Cached Transaction Attributes	Document	Document	M	M	M		
2.4.4	Interrupts	Document	Document	M	M	M		
2.4.5	Additional Transaction Attributes	Document	Document	M	M	M		
2.5	VC Interface							
2.5.1	User Guide	Document	Document	M	CM			If VCI is present
2.5.2	Implementation Guide	Document	Document	M	CM			If VCI is present
2.5.3	VC Interface Wrapper	VHDL, Verilog	VHDL, Verilog	M	CM			If VCI is present
2.5.4	Compliance Verification	Document	Document	M	CM			If VCI is present

Table 5: VSI Alliance Specification Test Specification (TST 1 1.1) Data Deliverables

Section	Deliverable	VSI Endorsed Formats	VSI Specified Formats	Soft	Firm	Hard	Comply ?	Comments
2.1.	Test Strategy							
2.1.1.	Description		Document	M	M	M		
2.1.2.	Test Completeness		Table	M	M	M		
2.1.3	Design-For- Test (DFT) Techniques			-	-	-		
2.1.3.1	SCAN		Document	CM	CM	CM		Conditional based upon VC provider's approach to achieve test coverage.
2.1.3.2	Logic Built-In Self Test (BIST)		Document	CM	CM	CM		Conditional based upon VC provider's approach to achieve test coverage.
2.1.3.3	Idd Quiescent Current (IDDQ Test)		Document	CM	CM	CM		Conditional based upon the requirements of the application being tested.
2.1.3.4	VC Isolation		Document	M	M	M		
2.1.3.5	Isolation Protocol		Document	CM	CM	CM		Conditional based upon the isolation technique chosen by the VC provider.
2.1.3.6	Test Collar		Document	CM	CM	CM		Conditional based upon the isolation technique chosen by the VC provider.
2.1.4	Test Strategy – Rationale		Document	-	-	-		Assignments not applicable.

Table 5: VSI Alliance Specification Test Specification (TST 1 1.1) Data Deliverables (Continued)

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Formats	Soft	Firm	Hard	Comply ?	Comments
2.1.5	Test Completeness – Rationale		Document	-	-	-		Assignments not applicable.
2.2.	Test Modules							
2.2.1	Target Use		Document	M	M	M		
2.2.2	Test Modes Utilized		Document	CM	CM	CM		Conditional based upon VC provider's decision to make available.
2.2.3	Implementation		Document, Table	M	M	M		
2.2.4	Fault Coverage		Document	CM	CM	CM		Not applicable to Test Modules yielding no results.
2.2.5	Constraints		Document	M	M	M		
2.2.6	Diagnostic or Characterization Information [Optional]		Document	CR	CR	CR		Optional additional information on makeup of Test Module.
2.2.7	Test Modules – Rationale		Document	-	-	-		Assignments not applicable.
2.3.	Test Modes							Test Modes created for design validation and not for test purposes are excluded.
2.3.1	Target Use		Document	CM	CM	CM		Availability based upon VC provider's willingness to disclose what may be proprietary information

Table 5: VSI Alliance Specification Test Specification (TST 1 1.1) Data Deliverables (Continued)

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Formats	Soft	Firm	Hard	Comply ?	Comments
2.3.2	Utilization		Document	CM	CM	CM		See 2.3.1 Comments above.
2.3.3	Constraints		Document	CM	CM	CM		See 2.3.1 Comments above.
2.3.4	Diagnostic or Characterization information [optional]		Document	CR	CR	CR		Optional additional information dependent upon Test Mode yielding a test result.
2.3.5	Test Mode – Rationale		Document	-	-	-		Assignments not applicable.
2.4.	Test vectors & Test Protocol							Applicable to all digital VCs except for memory oriented VCs, where algorithmic patterns are preferred.
2.4.1.	Test Vectors & Test Protocol Format	IEEE STIL	VCD, WGL	CM	CM	CM		Conditional based upon VC provider's choice.
2.4.2.	Waveforms		Timing Diagram	CM	CM	CM		Conditional based upon VC provider's approach to achieve test coverage.
2.4.3.	Timing Specification		Parameter Table	CM	CM	CM		Conditional based upon VC provider's approach to achieve test coverage.

Table 5: VSI Alliance Specification Test Specification (TST 1 1.1) Data Deliverables (Continued)

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Formats	Soft	Firm	Hard	Comply ?	Comments
2.4.4	Test vectors & Test Protocols – Rationale		Document	-	-	-		Assignments not applicable.
2.4.5	Waveforms and Timing Specifications – Rationale		Document	-	-	-		Assignments not applicable.

Table 6: VSI Alliance Specification (VCT 1 2.1) Data Deliverables

Section	Deliverable	VSIA Endorsed Formats	Soft	Firm	Hard	Comply ?	Comments
2.1	VC Provider Claims						
2.1.1	Functional Overview	ASCII, PDF, HTML	M	M	M		
2.1.2	Target Applications	ASCII, PDF, HTML	R	R	R		
2.1.3	Performance	ASCII, PDF, HTML	CM	CM	M		Provide for Soft & Firm if proven data from one or more implementation runs exists
2.1.4	Form Information	ASCII, PDF, HTML	M	M	M		
2.1.5	Test Coverage	ASCII, PDF, HTML	CM	CM	M		Provide for Soft & Firm if proven data from one or more implementation runs exists
2.1.6	List of Deliverables	ASCII, PDF, HTML	M	M	M		
2.1.7	Features and Standards Compliance	ASCII, PDF, HTML	M	M	M		
2.2	System Logic Description						
2.2.1	Functional Description	ASCII, PDF, HTML	M	M	M		
2.2.2	Structural Diagrams	ASCII, PDF, HTML	R	R	R		
2.2.3	Interfaces						
2.2.3.1	System- Level Interface	ASCII, PDF, HTML	M	M	M		
2.2.3.2	Logical (mapped) interfaces	ASCII, PDF, HTML	M	M	M		

Table 6: VSI Alliance Specification (VCT 1 2.1) Data Deliverables (Continued)

Section	Deliverable	VSI Endorsed Formats	Soft	Firm	Hard	Comply ?	Comments
2.2.4	Integration Requirements	ASCII, PDF, HTML	M	M	M		
2.2.5	Abstract Models	ASCII, PDF, HTML	R	R	R		
2.2.6	System/Logic Test Suite	ASCII, PDF, HTML	M	R	R		
2.3	Physical Description						
2.3.1	Interfaces		--	--			
2.3.1.1	Timing Specifications	ASCII, PDF, HTML	CR	CM	M		Supply for Soft and Firm if either have been repeatably implemented and consistent measurements are available
2.3.1.2	Electrical Characteristics	ASCII, PDF, HTML	CR	CM	M		(same as above)
2.3.2	Integration Requirements						
2.3.2.1	Clock Distribution	ASCII, PDF, HTML	N/A	R	M		Does not apply to Soft VC
2.3.2.2	Design Constraints	ASCII, PDF, HTML	CM	R	M		Only Global signal constraints apply to Soft
2.3.2.3	Design Compatibility	ASCII, PDF, HTML	CM	CM	M		For Soft and Firm, mandatory only for Schematic symbol library and design database format
2.3.2.4	Process Compatibility	ASCII, PDF, HTML	CR	CM	M		Supply for soft if data known from previous implementation; supply for Firm if hard aspects of Firm are known

Table 6: VSI Alliance Specification (VCT 1 2.1) Data Deliverables (Continued)

Section	Deliverable	VSIA Endorsed Formats	Soft	Firm	Hard	Comply ?	Comments
2.3.2.5	Process Requirements	ASCII, PDF, HTML	CR	CM	M		Supply for soft if data known from previous implementation; supply for Firm if hard aspects of Firm are known
2.3.2.6	Design Process Sensitivities	ASCII, PDF, HTML	CR	CM	M		Supply for soft if data known from previous implementation; supply for Firm if hard aspects of Firm are known
2.3.3	Implementation Test Suite	ASCII, PDF, HTML	M	M	M		
2.4	Reference Environment						
2.4.1	Verification of Claims	ASCII, PDF, HTML	M	M	M		
2.4.2	Tools, Flows & Methodology	ASCII, PDF, HTML	M	CM	CM		If a Tool, Flow, and/or Methodology applies to Firm and Hard, it must be supplied
2.4.3	ASIC Libraries	ASCII, PDF, HTML	CM	CM	CM		If ASIC Library has been used for any type (Soft, Firm or Hard) detail must be supplied
2.4.4	Process Technology	ASCII, PDF, HTML	CM	CM	M		If Soft and Firm have been implemented, information must be supplied
2.4.5	Naming Convention	ASCII, PDF, HTML	M	M	M		
2.4.6	Deliverables Documentation	ASCII, PDF, HTML	M	M	M		
2.5	Application Information						
2.5.1	Version History	ASCII, PDF, HTML	M	M	M		

Table 6: VSI Alliance Specification (VCT 1 2.1) Data Deliverables (Continued)

Section	Deliverable	VSI Endorsed Formats	Soft	Firm	Hard	Comply ?	Comments
2.5.2	Known Bugs	ASCII, PDF, HTML	M	M	M		
2.5.3	Application Notes		--	--			
2.5.3.1	Frequently Asked Questions	ASCII, PDF, HTML	R	R	R		
2.5.3.2	Design for Different Goals	ASCII, PDF, HTML	R	R	R		
2.5.3.3	Related/Family VC	ASCII, PDF, HTML	R	R	R		
2.5.3.4	Customization Options	ASCII, PDF, HTML	R	R	R		
2.5.3.5	Example Systems	ASCII, PDF, HTML	R	R	R		
2.6	Test Information						
2.6.1	Test Strategy	ASCII, PDF, HTML	CM	CM	M		For Soft and Firm strategy is applicable and should be supplied if equivalent to a prior existing implementation
2.6.2	Test Modules	ASCII, PDF, HTML	CM	CM	M		(same as Test Strategy)
2.6.3	Test Modes	ASCII, PDF, HTML	M	M	M		
2.6.4	Mixed Signal Test Integration	ASCII, PDF, HTML	--	--	--		
2.6.4.1	Signal Requirements for Analog Blocks	ASCII, PDF, HTML	N/A	N/A	CM		Not applicable to Soft or Firm and only applicable to Hard analog mixed signal VCs

Table 6: VSI Alliance Specification (VCT 1 2.1) Data Deliverables (Continued)

Section	Deliverable	VSI Endorsed Formats	Soft	Firm	Hard	Comply ?	Comments
2.6.4.2	Analog Test Requirements	ASCII, PDF, HTML	N/A	N/A	CM		Not applicable to Soft or Firm and only applicable to Hard analog mixed signal VCs
2.7	Supplier Information						
2.7.1	VC Provider Contact Information	ASCII, PDF, HTML	M	M	M		
2.7.2	Transfer Package Information	ASCII, PDF, HTML	M	M	M		
2.7.3	Standard Terms and Conditions	ASCII, PDF, HTML	M	M	M		
2.7.4	Third Party Reference		--	--	--		
2.7.4.1	Supporting VC Partner	ASCII, PDF, HTML	R	R	R		
2.7.4.2	ISV (Independent Software Vendor)	ASCII, PDF, HTML	R	R	R		

Table 7: VSI Alliance Specification Interface-Layer (IPP 1 1.0) Data Deliverables

Interface Abstraction Layer	IP Block Design Status			Commonly Used Formats	VSIA Format(s)
	Soft	Firm	Hard		
Layer 1.0	M	M	M	Document, C, C++, SDL	Document
Layer 0.x	R ⁽¹⁾	R ⁽¹⁾	R ⁽¹⁾	Document, C, C++, SDL	Document
Layer 0.0	M ⁽²⁾	M ⁽²⁾	M	Verilog, VHDL, Document	Document

3. Scope and Referenced IP

The intention of the VSIA is that all interface formats referenced in VSIA specifications must be open and available within the field of use defined by the specifications. To become an open standard format, the VSIA must determine that the interface is appropriate and the owner of the standard format must agree to open, non-discriminatory, and preferably royalty free terms.

This section addresses the deliverables that VC creators provide to VC integrators. At this time, the document does not address any issues regarding the generation (manual or automatic) of VCs. However, the deliverables created by a generator must meet the requirements of the VSIA Specification.

Table 8 lists the proprietary formats referenced in the Data Deliverables Tables and the owners of the formats.

Table 8: Proprietary Formats

Format	Description	Owner
DC Shell	Design Compiler Scripting Language	Synopsys
DEF	Design Exchange Format	Cadence
SPEF	Standard Parasitic Extended Format	Cadence
GDSII	Polygon Level Layout format	Cadence
ITL	Interpolated Table Lookup cell-level timing model	Mentor Graphics
LEF	Layout Exchange Format	Cadence
MMF	Motive Modeling Format	Viewlogic
NLDM	Non-Linear Delay Model cell-level timing model	Synopsys
TLF	Table Lookup Format – cell-level timing model	Cadence
VCD	Verilog Change Dump	Cadence
VCI Standard	VSI Alliance Virtual Component Interface Standard	VSI Alliance
WGL	Waveform Graphical Language	TSSI

3.1 DWG Specification Referenced IP

This section contains a copy of the Referenced IP sections of all the released specifications. The referenced IPs are listed by the Specification and Development Working Group.

3.1.1 System Level Design

To be released.

3.1.2 Manufacturing Related Test

This specification considers the following Intellectual Property:

Standard Test Interface Language (STIL): 1450

- Owner: IEEE/CS
- Status: Accredited standard

VCD (Verilog Change Dump): 1364-1995

- Owner: IEEE
- Status: Accredited standard

Embedded VC Test: P1500

- Owner: IEEE/CS
- Status: Standardization effort in progress. Anticipated in mid 2000.

3.1.3 IP Protection

To be released.

3.1.4 On Chip Busses

OCB 1 2.0

The only referenced IP in this specification are the open standard formats:

Verilog: IEEE 1364-1995

VHDL: IEEE 1076-198

C, and C++

VCI Standard: VSI Alliance Virtual Component Interface Standard

3.1.5 Analog/Mixed-Signal

AMS 1 2.1

This specification references a number of data formats, including:

VC Hspice: VC Hspice 1.0a

Owner: Avant! Corporation

Status: Licensed through Technology Contribution Agreement

<http://www.vsi.org>

VC LEF: VC LEF 5.1

Owner: Cadence Design Systems, Inc.

Status: Licensed through Technology Contribution Agreement

<http://www.vsi.org>

GDSII: GDSII Stream Format 6.0.0

Owner: Cadence Design Systems, Inc.

Status: Licensed through Technology Contribution Agreement

<http://www.vsi.org>

Verilog: IEEE 1364-1995

Owner: IEEE

Status: Accredited standard

<http://standards.ieee.org/faqs/order.html>

VHDL: IEEE 1076-1987

Owner: IEEE

Status: Accredited standard

<http://standards.ieee.org/faqs/order.html>

Verilog-AMS: Verilog-AMS Version 2.0¹

Owner: OVI

Status: Under development (Version 1.3 is an approved standard)

<http://www.oiv.org/>

VHDL-AMS: IEEE 1076.1-1999

Owner: IEEE

Status: Accredited standard

<Http://standards.ieee.org/faqs/order.html>

Open Library API (OLA)
Owner: OLA task force
Status: Under Development

<http://www.Si2.org/ola>

SPEF: IEEE P1481, 1998
Owner: IEEE
Status: IEEE Ballot Standard
<http://vhdl.org/vi/dpc/dpc-pandc/>

AMS 2 1.0
Spice: VC Hspice 1.0a (Spice)
Owner: Avant! Corporation
Status: Licensed through VSIA Technology Contribution Agreement
<http://www.vsi.org>

GDSII: GDSII Stream Format 6.0.0
Owner: Cadence Design Systems, Inc.
Status: Licensed through VSIA Technology Contribution Agreement
<http://www.vsi.org>

SPEF: IEEE P1481, 1998
Owner: IEEE
Status: IEEE Ballot Standard
<http://www.eda.org/dpc>

SDF: IEEE P1497
Owner: IEEE
Status: IEEE Ballot Standard
<http://www.eda.org/sdf>

VC LEF: VC LEF 5.1
Owner: Cadence Design Systems, Inc.
Status: Licensed through VSIA Technology Contribution Agreement
<http://www.vsi.org>

PDEF: IEEE P1481, 1998
Owner: IEEE
Status: IEEE Ballot Standard
<http://www.eda.org/dpc>

3.1.6 Implementation/Verification

I/V 1 2.1

This specification references several data formats, including:

Open Library API (OLA)

- Owner: OLA task force
- Status: under development
- <http://www.si2.org/ola>

Design Constraints Working Group (DC-WG)

- Owner: OVI
- Status: under development
- <http://www.vhdl.org/dcwg>

Verilog Synthesis Subset: IEEE 1364.1 Draft Standard Register Transfer Level Subset based on Verilog Hardware Description Language (the IEEE 1364.1 Draft specification is based on the OVI Verilog HDL Synthesis Subset specification)

- Owner: IEEE

- Status: IEEE Draft Standard
- <http://www.eda.org/vlog-synth>

VHDL Synthesis Subset: IEEE 1076.6 Draft Standard for VHDL Register Transfer Synthesis

- Owner: IEEE
- Status: IEEE Draft standard
- <http://standards.ieee.org/faqs/order.html>

Verilog: IEEE 1364-1995

- Owner: IEEE
- Status: Accredited standard
- <http://standards.ieee.org/faqs/order.html>

VHDL: IEEE 1076-1987

- Owner: IEEE
- Status: Accredited standard, older version
- <http://standards.ieee.org/faqs/order.html>

EDIF: EDIF 2 0 0

- Owner: EIA
- Status: Accredited standard, older version
- <http://www.edif.org/index.html>

Spice: VC Hspice 1.0a

- Owner: Avant! Corporation
- Status: Licensed through VSIA Technology Contribution Agreement
- <http://www.vsi.org>

SPEF: IEEE P1481, 1998

- Owner: IEEE
- Status: IEEE Ballot Standard
- <http://www.eda.org/dpc>

VC LEF: VC LEF 5.1

- Owner: Cadence Design Systems, Inc.
- Status: Licensed through VSIA Technology Contribution Agreement
- <http://www.vsi.org>

GDSII: GDSII Stream Format 6.0.0

- Owner: Cadence Design Systems, Inc.
- Status: Licensed through VSIA Technology Contribution Agreement
- <http://www.vsi.org>

3.1.7 VC Transfer

VCT 1 2.1

This document contains no specifically referenced IP.

3.2 DWG Specification Scopes

The following sections are the “Scope” sections of the individual specifications. The “Scope” section defines the area of applicability of that specification, it may still require interpretation for each individual VC, depending on its individual characteristics. Refer to the scope sections below, or the Specification Data Sheets to determine its applicability to your particular VC.

3.2.1 System Level Design

To be released.

3.2.2 Manufacturing Related Test

TST 1 1.1

This specification covers Test Data Interchange formats and Design-For-Test (DFT) Guidelines for VC providers. Its purpose is to define the nature and format of the information transferred between the VC Provider and the VC integrator. Guidelines for VC providers are also presented, to insure successful incorporation of Virtual Components (VCs) into a system chip design using the VSIA (Virtual Socket Interface Alliance) methodology. All test related information from the VSIA Architecture Document (including section 1.5) and test guidelines from Section 3 are covered. Subsequent revisions of this document will cover the transfer of similar information between the VC integrator and the manufacturing Test Engineering function.

The “field of use” for VSIA standard formats is defined as creating, defining, exchanging and integrating descriptions of virtual components of integrated circuits.

3.2.3 IP Protection

To be released.

3.2.4 On Chip Bus

OCB 1 2.0

This specification applies to on-chip buses and their supporting material, which could be classified as system buses or peripheral buses in accordance with the definitions in this document.

3.2.5 Analog/Mixed-Signal

AMS 1 2.1

The scope of this document is to specify deliverables, their associated design guidelines, and data formats to facilitate the test, exchange, and integration of process specific (“hard”) mixed-signal virtual components. These components target largely digital system chip applications.

This document also provides a detailed deliverables list of models to assist the exchange, integration, and verification of process specific (“hard”) mixed-signal virtual components.

The “field of use” for VSIA standard data formats is defined as creating, defining, exchanging, and integrating descriptions of virtual components (VCs) of integrated circuits.

AMS 2 1.0

The scope of this document is to specify and explain deliverables, data formats, associated design guidelines, and example designs for the signal-integrity (SI) issues of both digital and analog mixed-signal virtual components (VC) in SoC design.

This specification is focused on SI issues in the communication between the VC authors and integrators for the integration of Digital and Analog Mixed-Signal blocks (VC) in SoC designs, including design of the interface. It is assumed that the virtual components are provided for integration as hard blocks.

3.2.6 Implementation/Verification

I/V 1 2.1

This specification defines the VC data representation standards to support the hardware design flow from RTL design planning through final verification.

This specification includes the RTL source and performance model formats needed for both hard and soft VCs, summary of the design constraints requirements, endorsement of the OVI Design Constraints Working Group (DC-WG) for the development of the design constraints standard, append “API” to Open Library to give Open Library API, and the endorsement of the Open Library (OLA) standard for the performance modeling standard.

The specification includes the data formats that should be used for the structural netlist and a number of physical data types associated with hard VCs. The specification also includes a set of guidelines for reducing the likelihood of name-space collisions between different VCs, and between VCs and other system logic, as well as guidelines for handling any name-space collisions that do occur.

The “field of use” for VSIA standard data formats is defined as creating, defining, exchanging, and integrating descriptions of virtual components of integrated circuits.

3.2.7 VC Transfer

VCT 2 2.0

The VCT Functional Classification scheme facilitates the search process by providing a framework for the consistent definition of values for the functional class attribute (ClassClassification). The specific choices for each name used in this classification scheme were arrived at after a careful examination of functional taxonomies from Cadence, Design & Reuse, IP Highway, RAPID, and Toshiba. There is no limitation mandate as to the use of the VCT Functional Classification. A VC can be attached to more than one functional class if necessary for complete coverage of its possible functions.

The top and second levels contain an Others class for use in cases where the specific VC does not readily fit into any existing named category. As industry usage warrants, and it becomes appropriate to expand the classification scheme, new functional classes will be added to accommodate popular new functions.

3.2.8 VC Quality

To be released.

3.2.9 Hardware-dependent Software

To be released.

4. Endorsements

The VSIA DWGs will work with other standards organizations for the development of new or emerging standards required for implementation and verification of VCs and system chip integration. The VSIA DWG may endorse the development of select standards provided the DWG requirements are included in the development of the standard. The standard will be specified by the DWG when the standard is completed, approved by the standard organization and meets the DWG requirements.

The purpose of the endorsements are to allow VC providers, system integrators and EDA developers to prepare development plans needed to support the future adoption of these emerging standards.

The following outlines the DWG specification and endorsement process:

- Define the VSIA requirements for the integration/verification of VCs.
- Identify potential defacto, accredited, or emerging standards.
- Work with standards organization to endorse the emerging standard if defacto or accredited standards are not available or sufficient.
 - Encourage participation from VSIA members and industry.
 - Provide VSIA inputs and requirements necessary for the development of the standard.
 - Endorse the standard development, if the VSIA requirements are included.
 - Participate in the reviews of the draft standard.
 - Specify the standard for the VSIA specification when the standard is completed and approved, provided it meets the VSIA requirements.
 - Promote the use of the standard.

4.1 Design Constraints Endorsement

The I/V DWG endorses the OVI Design Constraints Working Group (DC-WG) development of a Design Constraints standard. The I/V DWG is working with the OVI DC-WG to define the group charter, scope, and requirements. The design constraint requirements are specified in Section 2.4 of the *I/V 1 2.0 Specification (Soft and Hard VC Structural, Performance and Physical Modeling Specification)*.

4.2 Performance Modeling Endorsement

The performance modeling and library attribute data requires advanced features and capabilities to support the emerging very deep sub-micron process and design technologies. The I/V DWG endorses the development of the Open Library API (OLA) standard to provide the advanced capabilities needed to support the emerging technologies. We strongly encourage the development of the OLA standard, OLA based EDA tools, and ASIC libraries to provide the infrastructure needed for the production deployment of OLA for VC deliverables, and system chip design, and verification.

Table 3 lists the criteria to define the requirements and dependencies necessary for the production deployment of OLA. They are based on when VC providers and system chip designers can effectively use OLA for VC exchange and system chip design. The criteria define the specific VSIA trigger points and target time frame for the adoption of OLA as a VSIA standard. The criteria will be monitored and the target time frame will be updated accordingly.

Table 9: OLA Requirements and Dependencies

Criteria	Requirements	Summary
Technical Suitability	The OLA standard must support the requirements for the Performance Models. Trigger: Standard needs to meet the VSIA requirements.	The OLA is an API based standard and is a combination of DCL for delay calculation and ALF for function and attribute specification.
Process Technology	The advanced process technologies will be one of the primary drivers for the adoption of OLA. Trigger: Production availability of the advanced .25 and .15 um process technologies.	The modeling requirements for the advanced .25 and .15 um technologies will drive the need and use of OLA. It is expected the .5 and .35 um technologies will continue to use the existing formats.
ASIC Library availability	ASIC libraries supporting OLA is a key OLA infrastructure requirement for the VC and system chip integration. Trigger: Availability of a significant number of OLA ASIC libraries for a specific generation of process technology.	The initial set of production ASIC OLA libraries will be available by Q1 1999.
EDA tool support	Mainstream EDA tool support of OLA is also a key OLA infrastructure requirement for VC and system chip integration. Trigger: EDA tools that support a significant number of design flows.	The initial set of EDA tools supporting OLA is expected to be released by the end of 1998.
Standard availability	The specification of the OLA standard is required. Trigger: Completed specification that includes the VSIA requirements.	The initial OLA draft standard is expected to be available by the end of 1998. The initial version of the standard may not include all the necessary requirements.
DWG Sponsored Pilot	A DWG sponsored pilot will be required to validate that OLA can be utilized for VC and system chip integration. Trigger: Completion of DWG sponsored pilot.	The pilot needs to address applicability of OLA to complex IP functions, VC functions from multiple sources, integration of interconnect delay algorithm, and complex delivery and support mechanism.

A. References

A.1 Open Standards References

The following list the open standard references:

- IEEE Std 1076-1987, IEEE Standard VHDL Language Reference Manual.
IEEE Std 1076-1987 is no longer in print and is NOT available from the IEEE.
- ANSI/IEEE Std 1076-1993 (Revision of IEEE Std 1076-1987), IEEE Standard VHDL Language Reference Manual.
IEEE Std 1076-1993 has superseded IEEE Std 1076-1987.
- IEEE Std 1164-1993, IEEE Standard Multivalued Logic System for VHDL Model Interoperability (Std_logic_1164).1
IEEE Std 1164-1993 provides a portable, industry standard simulation environment for VHDL coders.
- IEEE Std 1364, Verilog Hardware Description Language Reference Manual.
- OVI Standard Delay Format (SDF) Specification, Version 2.1-3.0.
- OVI-CFI Standard Delay Calculation System Specification, Version 1.0.
- ISO/IEC 9899-1990, The Programming Language C.

All IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

ANSI publications are available from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.

All OVI publications are available from Open Verilog International (OVI), 15466 Los Gatos Blvd., Suite 109-071, Los Gatos, CA 95032.

All CFI publications are available from CFI, 4030 West Braker Lane, Suite 550, Austin, TX 78759, USA

A.2 VSIA Reference Documents

The following are VSIA reference documents:

- VSIA Architecture Document 1.0
- System-Level Design Model Taxonomy (SLD 2.2.x)
- Taxonomy of Functional Verification for Virtual Component Development and Integration (VER 1.1.x)

All VSIA publications are available from the VSI Alliance Web site at www.vsi.org.

B. Glossary of Terms

B.1 Acknowledgments

The VSIA acknowledges the contribution by Lockheed Martin Advanced Technology Laboratories for the basis of the underlying document *RASSP VHDL Modeling Terminology and Taxonomy*, Revision 2.3, June 23, 1997, which has been the source of several definitions in this glossary. The RASSP document was developed jointly under the DARPA/Tri-Services “Rapid Prototyping of Application Specific Signal Processors” (RASSP) program by Lockheed Martin Advanced Technology Laboratories, DARPA/Tri-Services, South Carolina Research Authority, Lockheed Sanders, Honeywell Technology Center and Georgia Institute School of Electrical & Computer Engineering.

B.2 Rationale and Purpose

Differing terminology has the potential of creating confusion within the system-chip industry. Some groups use common terms with divergent meanings, while others use different words for the same thing. Clear communication in common semantics is important to achieving the goals of the Virtual Socket Interface Alliance (VSIA).

This glossary is a compilation of relevant and specific terms for VSIA members. The intent is to focus on those terms, required for the efficient authoring and integration of VCs. Many of the terms have been defined by the VSIA and are represented in the Architecture Document. Others have been borrowed from industry sources (with permission when needed). Overlap and conflict may be noted in some terms, which is appropriate at this emerging point in the VC industry and is one of the reasons for publishing this information. Contributions to the terminology family should be shared and discussed. Agreement on appropriate descriptive words and their definitions is desired.

The purpose of this glossary is threefold:

- To make, the terminology relevant to the work of the VSIA publicly available.
- To provide a mechanism for refinement of relevant terminology.
- To enable the standardization of relevant terminology, informally and formally.

Input from the Development Working Groups, for terms of unique semantic import, will continue to be added. Comments on DWG-specific terminology should be directed to the DWG chairperson.

B.3 Attribution Reference

Definitions that can be attributed to a source contain a reference of the form:

[Source, Scope] where:

Source is the name of the individual or organization that provided the definition. Member, when used in the Attribution, denotes a member of VSIA.

Scope is one of the following:

- General (an industry wide term)
- VSIA (a VSIA specific term)
- DWG name (SLD, TST, IPP, OCB, AMS, I/V, VCT, Ver) and document revision (x x.x)

B.4 Definition of Terms

Table 10: Definition of Terms

A/D	Analog-to-Digital (converter)
Address Spaces	A reference to the separate physical address regions such as: memory, I/O, and configuration.
Advanced Packet Model	A packet model where request and response may have different number of cells.
Agent	An entity that operates on a computer bus.
Application Layer	This layer deals with the software components in a bus transfer, the driver, OS interface, and specific user application.
Arbitration Hiding	Mechanism to give advance information to the arbitration logic to prevent arbitration cycles adding latency to VCI operation.
Arbitration Latency	The time that the master waits after having asserted request until it receives grant and the bus returns to the idle state after the previous master's transaction.
Architecture	<p>In general, the structure of anything.</p> <p>In the context of Software Architecture, it is the configuration of all software routines and services for meeting a system objective.</p> <p>In the context of Hardware Architecture, it is the configuration of all physical elements for meeting a system objective.</p> <p>In the context of System Architecture, is the collection and relationship of the system's constituent hardware and software components. For example, a multi-processor system architecture would include the hardware network architecture and the software architecture in the form of distributed and local operating systems, application routines, and control routines. [RASSP, SLD DWG]</p>
Artisan	A provider of foundation IP
Artiscan(tm)	Software implementation of the VSIA tagging standard and reporting mechanism; available to Artisan's semiconductor partners.
Atomic	Defines a property on an interface action. An atomic action either completes fully or not at all. An atomic action that completes fully does so without the possibility of interruption or interference. If an atomic action does not complete fully (that is, it is abandoned) then the state of the system must be as if the action had never started.
Attributes	These are some classifications by which the behaviors of objects can be more specifically defined. For example, a basic transaction may be a read and an attribute on that read could be blocking.
Authoring	A process by which a block is designed to conform to a set of specifications. The output should be in the standard format with a pre-defined set of characteristics, which will simplify integration and verification. Also termed "block creation." [VSI Alliance, VSIA]
Basic Delay Model	Defines timing specification of the VC.
Behavioral Blocks	The behavioral entities that correspond to components stripped of their interface protocols are referred to as "behavioral Blocks."

Table 10: Definition of Terms (Continued)

Behavioral Model	A description of the function and timing of a component without describing a specific implementation. A behavioral model can exist at any level of abstraction. Abstraction depends on the precision of implementation details. For example, a behavior model can be a model that describes the bulk time and functionality of a processor that executes an abstract algorithm, or it can be a model of the processor at the less abstract instructions-set level. The precision of internal and external data values depends on the model's abstraction level. [RASSP, SLD DWG]
BIST Register	An optional Built-in Self Test register in the header region used for control and status of built-in self-tests.
Black Box	An implementation of a hard, firm, or soft VC (see below) that is hidden from the designer. It is only observable as a bus functional model at the I/O ports. [Dataquest, General]
Block	A pre-implemented, reusable module of intellectual property that can be quickly inserted and verified to create a single-chip system. Also called megacells or cores. [Member, VSIA]
Bridge	The logic that connects one computer bus to another, allowing an agent on one bus to access an agent on the other.
Burst Transfer	The basic bus transfer mechanism. A burst is comprised of an address phase and one or more data phases.
Bus Commands	Signals used to indicate to a target the type of transaction the master is requesting.
Bus Hierarchy	The structure and interconnection of busses within a System IC. Typically the order of the busses is from the processor out. The processor bus is connected to the System or Local bus, which is connected, via a bridge to the Peripheral bus. [Member, OCB DWG]
Bus Transfer Level	This deals with the protocols used to transfer words between two components across a bus, within the time frame of a few clock cycles.
Bus Wrapper	A virtual component interface between the bus interface logic and a virtual component that is independent of the specific bus protocol. [Member, OCB DWG]
Cell	A grouping of one or more bytes. It contains a number of bytes that is characteristic to the natural width of the VCI implementation. It is the basic unit of information transferred across the VCI in one cycle.
Cell Level Netlist	A structural interconnection of design objects ranging from simple logic gates to complex functions.
Central Resources	Bus support functions supplied by the host system.
Channel	The connectivity mechanism between any two components. Each channel has associated attributes along with its behavior. A channel may be specified at multiple levels of abstraction.
Circuit Level Netlist	A structural interconnection of semiconductor devices such as transistors, resistors, and capacitors.
Clean Snoop	A snoop that does not result in a cache providing modified data.
Configuration Address	A set of registers used for configuration, initialization, and catastrophic

Table 10: Definition of Terms (Continued)

Configuration Cycle	Bus cycles used for system initialization and configuration via the configuration address space.
Cores	A complex, pre-designed function that is to be integrated onto a larger chip. Examples are PCI, MPEG, and DSP functions as well as 8-, 16-, and 32-bit microprocessors and microcontrollers. [Member, General]
Crosstalk	Any deviation from the ideal signal waveform propagating in an interconnect wire caused by signal transitions in other wires in the neighborhood.
Datum	A datum is a primitive object which is one of the data types documented in the SLI behavioral Document Standard. Data may be transmitted through interface ports by transport objects like Messages and be acted upon by behavior objects like Protocol blocks.
Defects	Specific flaws, physical, or chemical imperfections on a manufactured device. Most defects can be detected and measured by a FA group. Specific devices that do not perform as expected contain defect(s) or have design flaws. [Member, TST 1 1.0]
Delayed Transaction	The process of a target latching a request and completing it after the master was terminated with retry.
Equivalence Verification	Process of determining whether multiple levels or formats of a design match in terms of functionality.
Fault Coverage	A measure that defines the percentage of success a test set has in finding simulated “stuck at 0” or “stuck at 1” faults for a list of nodes in a given design. It may be extended to other fault model types. A general definition of fault coverage is the percentage of all faults checked on a particular fault model. The coverage measure should be given for each model type tested. As the user defines the nodes to be evaluated (in some cases this is done by defining lists of nodes not to be used in the task), the raw number has little meaning without a full analysis of the set up. [VSI Alliance, General]
Faults	Refers to classes or concepts of defect types. The most common of these is the “stuck at” type fault class. In the EDA and academic worlds, a fault is a software model of a defect. [VSI Alliance, VSIA]
Firm VC	VCS that have been structurally and topologically optimized for performance and area through floorplanning or placement using a generic technology library. The level of detail ranges from region placement of RTL sub-blocks, to relatively placed datapaths, to parameterized generators, to a fully placed netlist. Often a combination of these approaches is used to meet the design goals. Firm VCs offer a compromise between Soft VCs and Hard VCs. They are more flexible and portable than Hard VCs, yet more predictive of performance and area than Soft VCs. Firm VCs include a combination of synthesizable RTL, reference technology library, detailed floorplan, and a full or partial netlist. When a full netlist is present, it is expected that the test logic has been inserted and that the test lists will accompany the design. Firm VCs do not include routing. Protection risk is equivalent to Soft. [VSI Alliance, VSIA]

Table 10: Definition of Terms (Continued)

Functional Model	A model that describes the function of a system or component without describing a specific implementation. A functional model can exist at any level of abstraction. Abstraction depends on the precision of implementation details. For example, a functional model can be a model that abstractly describes the function of a signal processing algorithm, or it can be a less abstract model that describes the function of an ALU for accomplishing the algorithm. The precision of internal and external data values depends on the model's abstraction level. [RASSP, SLD DWG]
Gray Box	Includes additional details of the internal structure so tools using the model can more accurately analyze the effect of the environment around the VC.
Hard Blocks	A GDSII-Stream representation of a virtual component
Hard VC	VCS that have been optimized for power, size, or performance and mapped to a specific technology. Examples include netlists fully placed, routed, and optimized for a specific technology library, a custom physical layout, or a combination of the two. Hard VCs are process/vendor specific and generally expressed in GDSII format. They have the advantage of being much more predictable, but consequently are less flexible and portable due to process dependencies. Hard VCs require, at a minimum, a high-level behavioral model, a test list, full physical and timing models along with the GDSII data. The ability to legally protect Hard VCs is much better because there is no requirement for RTL. [VSI Alliance, VSIA]
Header Region	A region of fields that uniquely identify a device and allow the device to be generically controlled.
Hidden Arbitration	Arbitration that occurs during a previous access so that no bus cycles are consumed by arbitration, except when the bus is idle.
Host Bus Bridge	A low latency path through which the processor may directly access devices mapped anywhere in the memory, I/O, or configuration address spaces.
HW/SW Co-Design	A design methodology supporting the concurrent development of hardware and software to achieve system functionality and performance goals. In particular, “co-design” often refers to design activities prior to the partitioning into Hardware and Software and the activity of design partitioning itself. [Member, SLD DWG]
HW/SW Co-Simulation	A process by which the software is verified against a simulated representation of the hardware prior to lab or system integration. [Mancini et al, DAC 95, p. 522, SLD DWG]
HW/SW Co-Verification	Refers to all verification activities for mixed hardware-software systems that occur after the explicit partitioning into hardware and software components, and which involve an explicit representation of both hardware and software elements. Co-verification involves both formal verification and simulation-based techniques and methodologies. It also encompasses the verification activities that use integrated lab system prototypes. [Member, SLD DWG]
Idle state	Any clock period that the bus is idle.
Initiator	A VC that sends request packets and receives response packets. It is the agent that initiates transactions, for example, DMA.
Integration Verification	Process of verifying the functionality of a system-on-chip (SoC) design that contains one or more virtual components.

Table 10: Definition of Terms (Continued)

Intellectual Property	A term encompassing all products, technology, software, and so forth that have been
Intent Verification	Process of determining whether a design fulfills a specification of its behavior.
Interface	An interface to a component is the sum of all communication-both implicit and explicit-between that component and everything else. It may include not only the static types and sizes of ports, but also the definition of the entire protocol necessary to communicate with a specific instantiation of the component. The interface may define a protocol at many levels of abstraction. These levels must be consistent with each other so that the capabilities of the communication protocol observed at one level of abstraction hold at all levels of abstraction below that. An interface to a virtual component consists of a set of channels and the protocols defined on these channels. The point at which a channel connects to a component is known as a port.
Interface Abstraction Layers / Levels	These are the differing levels of protocol specification that may accompany an interface description. Depending upon the type of interface, certain properties suitable for the description of each layer may be specified. Levels of abstraction on interfaces may be used for: data (for example from enumeration to bit mask) communication (for example from point-to-point to bus communication or from transaction level to messages to cells) resource (for example infinite buffer and non blocking to fixed register and blocking) time (for example data flow to serial processes to clocked)
Interface Model	A component model that describes the operation of a component with respect to its surrounding environment. The external port-structure, functional, and timing details of the interface are provided to show how the component exchanges information with its environment. An interface model contains no details about the internal structure, function, data values, or timing other than that necessary to accurately model the external interface behavior. External data values are usually not modeled unless they represent control information. An interface model may describe interface details of a component at any level of abstraction. The term, “bus functional” and “interface behavioral” have also been used to refer to an interface model and are considered synonyms. The more general interface model name is preferred to the anachronistic term “bus functional.” [RASSP, SLD DWG]
Internal Test Logic	Refers to the test logic included with the VC or can be included within the VC by the user to facilitate test generation of vectors for the VC. [VSI Alliance, VSIA]
Interoperability	Model interoperability designates the degree to which one model may be connected to other models, and have them function properly, with a modicum of effort. Model interoperability requires agreement in interface structure, data format, timing, protocol, and the information content/semantics of exchanged signals.
Keepers	Another name for pull-up resistors that are only used to sustain a signal state.
Latency	<i>See</i> arbitration latency, master data latency, target initial latency, target subsequent latency.
Latency Timer	A mechanism for ensuring that a bus master does not extend the access latency of other masters beyond a specified value.
Layer	A vertical segmentation of the process of transferring information across buses. There are four relevant levels: application layer, transaction layer, bus transfer layer, and physical layer.

Table 10: Definition of Terms (Continued)

Livelock	A condition in which two or more operations require completion of another operation before they can complete.
Local Bus	A bus that connects between the processor and high-speed peripheral functions such as a memory controller, an off chip bus, etc. (See System Bus) [Member, OCB DWG]
Manufacturing Test	A term used by the Manufacturing-Related Test DWG to convey completeness. It encompasses all ATE test-related activities by VC providers, VC integrators, and semiconductor, fab/assembly/test providers. Manufacturing Test is the physical process of validating and debugging the performance and functional operation of semiconductor products. Physical testing over the manufacturing lifetime of a device includes (but is not limited to) validation, characterization, production test, and failure analysis. [VSI Alliance, General]
Master	An agent that initiates a bus transaction.
Master Data Latency	The number of clocks until ready is asserted.
Master-Abort	A termination mechanism that allows a master to terminate a transaction when no target responds.
Messages	A message is an atomic transport object that transfers zero or more cells or data in the same direction to or from a port.
Miller Coupling Factor	In the context of interconnects, the multiplier used for the capacitive coupling from neighboring wires to account for the impact on the delay because of their simultaneous switching.
Model (PIN)	Specifies the interconnection RCs for the peripheral interconnect between the physical I/O ports and the internal gates of the VC.
Model (RTL)	An RTL model describes a system in terms of registers, combinational circuitry, low-level buses, and control circuits, usually implemented as finite state machines. Some internal structural implementation formation is implied by the register transformations, but this information is not explicitly described. The primary purpose of RTL models is for developing and testing the internal architecture and control logic within an IC component so the design satisfies the required functionality and timing constraints of the IC. The RTL model is also used for specifying the design in a process neutral format that is retargetable to specific technologies or process lines through automatic synthesis. It is often used for the generating detailed test vectors, gathering timing measurements to increase the accuracy of more abstract models, investigating interactions with closely connected components, and it unambiguously documents the design solution.
Motherboard	A circuit board containing the basic functions (e.g., CPU, memory, I/O, and expansion connectors) of a computer.
Mutex	A logical guarantee of the mutual exclusivity of the transitions of two signals.
One hot	A set of signals such that exactly one of them is active at any instant.
Operation	A specialized transport object consisting of a pair of packets, which are usually transferred in different directions, for example, a request packet and a response packet. A logical sequence of transactions, for example, Lock.
Packet	A transport object consisting of a group of cells transferred across the VC Interface.

Table 10: Definition of Terms (Continued)

Packet Chain	A non-atomic specialized transport object consisting of a set of logically connected packets transferred in the same direction across a VC Interface. The chain of packets is connected because no intervening packets are allowed on the same channel.
Performance Model	A collection of the measures of quality of a design that relates to the timely response of the system in reacting to stimuli. Measures associated with performance include response time, throughput, and utilization. A performance model may be written at any level of abstraction. In general, a performance model may describe the time required to perform simple tasks such as, memory access of a single CPU. However, in the context of VSIA, the typical abstraction level for performance models is most often at the multiprocessor network level. [RASSP, SLD DWG]
Peripheral Bus	A slower speed, simpler bus that is used for serial and slow speed devices. It is generally connected to the System or Local bus through a bus bridge. [Member, OCB DWG]
Peripheral Interconnect Model (PIM)	Specifies the interconnection RCs for the peripheral interconnect between the physical I/O ports and the internal gates of the VC.
Phase 1	One or more clocks in which a single unit of information is transferred, consisting of:
Phase 2	An <i>address phase</i> (a single address transfer in one clock for a single address cycle and two clocks for a dual address cycle).
Phase 3	A <i>data phase</i> (one transfer state plus zero or more wait states).
Physical Blocks	A model of the physical implementation of the VC and the system chip.
Physical Prototype	A physical model of a product, component, or system. The traditional prototype is a physical prototype, in comparison to a virtual prototype. See prototype, virtual prototype. [RASSP, SLD DWG]
Physical Verification	Physical verification is the process of checking the geometric design database to ensure that the physical implementation is a correct representation of the original logic design. Physical verification consists of three distinct checks: Electrical Rules Checks (ERC), Design Rules Checks (DRC) and Layout Versus Schematic Checks (LVS).
Platform	The underlying enabling technology on which the object of reference is rendered functional. This can extend to the capabilities of engineering, support, and sales teams. [VCT 1 2.0]
Port	Refers to a set of signals that reside on the boundary of a VC. A port is a connectable point on the VC through which information may travel. A port may have specified attributes and constraints that can range from the direction and size of the port to the definition of the behavioral principle of the port (such as blocking-read) to the specification of the protocol in which the port performs a role[VCT 1 2.0]
Positive Decoding	A method of address decoding in which a device responds to accesses only within an assigned address range. (<i>See also</i> subtractive decoding)
Power Model	Defines the power specification of the VC.

Table 10: Definition of Terms (Continued)

Processor Bus	A bus that connects the internal components of the processor together. Typically these are the cache, instruction, and the execution units. It also has an external connection to the System or Local bus. It is proprietary and tightly coupled with the processor architecture. [Member, OCB DWG]
Protocol	The specification of the communications etiquette. A protocol may include the specification of the control lines and their behavior and relationship to data, the specification of the data types and their values (if necessary), communication timing, state (if implied by the communication semantics), and so on.
Protocol Blocks	The specification of how a set of transport objects and their data combine and cooperate to perform a higher-level task. They can be thought of as "pattern mappings" from one layer of abstraction to another.
Protocol Checkers	A means for checking behavior of an interface and determining if violations of defined, acceptable behavior have occurred.
Prototype	A preliminary working example or model of a product, component, or system. It is often abstract or lacking in some details from the final version. Two classes of prototypes are used in the design process: physical prototypes and virtual prototypes. The purpose of a prototype is for testing, exploration, demonstration, validation, and as a design aid. It is used for testing design concepts and exploring design alternatives. Prototypes are also used to demonstrate design solutions or validate design features. [RASSP, SLD DWG]
Random Pattern Simulation	A simulation in which randomly chosen address, data and control values are driven onto a bus or other circuit elements.
Reconfigurable Prototyping System	A system in which virtual components (VCs) of a system-on-chip (SoC) design are created in off-the-shelf components, bonded-out silicon, FPGAs or in-circuit emulator systems.
Register Transfer Language (RTL)	A programming language representation of a design in which some, but not all of the design structure is explicitly represented. Both the Verilog and VHDL languages are used for RTL modeling.
Register Transfer Level	
Regression Testing	Techniques for running large numbers of simulations in batch mode, with minimal human intervention. Also, results are analyzed in batch mode, and fails are reported in an automatic way.
Retract	A form of abort from the initiating side of the transaction.
Retry	A transaction that was stopped, and is then reinitiated anew.
Reusable Component	A design object. This refers to the type of component for which a physical implementation exists that can be re-used. For example, ALU chips or macrocells that can be embedded in larger chips, etc. These designs are largely implemented in specific technologies. Limited parameterization may be possible. These design objects typically exist in technology libraries from one or more suppliers. [EDA Industry Standards Roadmap 1996 - http://www.cfi.org/roadmap/BOOK.html , General]

Table 10: Definition of Terms (Continued)

Reusable Design Object	
Reusable Function	A design object that refers to the concept of a simulatable design specification for the design object that can be reused. The examples here might start with ALU chips or entire microprocessor designs for which a VHDL or Verilog simulation model is available. This type of reusable design object is used to enable simulation of a candidate object in a new design context or to develop a new physical technology implementation of a previously designed function. [EDA Industry Standards Roadmap 1996 - http://www.cfi.org/roadmap/BOOK.html , General]
RTL Source	Defines the VC source description and is the primary input for the implementation and verification of the VC within a system chip design.
RTL to Netlist Test Suite Migration	A means for translating a test suite that operated on the RTL level to one that operates on the netlist level of a design.
Semi-Formal Verification	Techniques which use simulation results as the starting point for formal techniques. These techniques typically explore only a portion of a state space and are therefore less exhaustive than model checking.
Sequential Equivalence Checking	Formal equivalency checking techniques that do not rely on mapping of memory elements in one design to another, but rather prove that designs with different numbers of, or different arrangements of, memory elements produce the same output streams given the same input streams. Normally, a set of initial states for each of the designs must be specified.
Shadow Logic	User defined logic (UDL) accessible only from the input/output ports of VCs. Such a VC is thought of as casting a shadow, which potentially reduces the testability of the logic in that shadow. The addition of test access to the VC ports is said to cast light on or remove the shadow. If the UDL contains internal test access points (such as scan elements, which can act as both test control and test observation points), then the shadow logic includes only the logic between the VC output ports. And the first level of test (control) access points in the UDL and the logic between the last level of test (observation) access points in the UDL and the VC input ports. Shadow logic that is partially accessible from other non-shadowed UDL through chip primary ports or test access points in the UDL is sometimes said to be partially shadowed since the ease of detecting faults on some logic nodes in the shadow logic may be unaffected because of this partial accessibility. Simple logic (such as buffers and inverters) in the interconnect between VCs is said to be trivial shadow logic and may be considered only during interconnect testing. [Member, TST 1 1.0]
Signal	Synonymous to electrical wire or net.
Signal Coverage	Shows how well state signals or ROM addresses have been exercised.
System-Level Integration	A System Level Integration (SLI) device, also known as system-on-silicon, is a device with greater than 100k gates with at least one programmable core and on-chip memory. [Dataquest, General]
Slew	The slope of a digital signal propagating in an interconnect (in voltage change per unit time).
Snarf	Similar to snooping, a module is said to snarf a transaction if it takes a copy of data passing by on the bus even though it did not request it.

Table 10: Definition of Terms (Continued)

Socket Test Interface	Describes the way the VC can be individually accessed from the chip I/O for testing. [VSI Alliance, TST 1 1.0]
Soft Core	A non-physical (i.e., not GDSII-Stream) view of a virtual component
Soft VC	VCS that are delivered in the form of synthesizable HDL code. The advantage is the flexibility of the source code so it can be retargeted to multiple manufacturing processes. The disadvantage is the difficulty in performance prediction (such as timing, area, and power). Soft VCs typically have higher intellectual property protection risks because RTL source code is required by the integrator. [VSI Alliance, VSIA]
Source Code	A completely open VC. [Dataquest, General]
Space	error handling.
Special Cycle	A message broadcast mechanism used for communicating processor status and/or (optionally) logical sideband signaling between agents.
Specification	A specification comprised of many “datasheets” or design object specification-related information about a reusable object. This information base is the initial access point for the library of reusable design objects. It is used to help designers determine the existence of a reusable design object that can be reused in a new design situation. Typically, a Design Object Specification would exist if, and only if, one of the reusable function or component design objects also exists. [EDA Industry Standards Roadmap 1996 - http://www.cfi.org/roadmap/BOOK.html , General]
Split Transaction	A transaction that is ended incomplete, usually to complete some other transaction, and then re-established to complete.
Stale Data	Data in a cache-based system that is no longer valid and, therefore, must be discarded.
Statement Coverage	Coverage method for showing how many times a statement in the RTL was executed.
Static Functional Verification	Static functional verification exploits formal mathematical techniques to verify a design without the use of verification test suites. There is no industry consensus on the verification approaches included under this term.
Stepping	The ability of an agent to spread assertion of qualified signals over several clocks.
Structural Model	A representation of a component or system in terms of the interconnections of its constituent components. A structural model follows the physical hierarchy of the system. The hierarchy reflects the physical organization of a specific implementation. A structural model describes the physical structure of a specific implementation by specifying the components and their topological interconnections. These components can be described structurally, functionally, or behaviorally. Simulation of a structural model requires all models in the lowest (leaf) branches of the hierarchy to be behavioral or functional models. Therefore, the effective temporal, data value, and functional precisions depend on the leaf models. A structural model can exist at any level of abstraction. Structural precision depends on the granularity of the structural blocks. [RASSP, SLD DWG]
Subtractive Decoding	A method of address decoding in which a device accepts all accesses not positively decoded by another agent. (<i>See also</i> positive decoding)

Table 10: Definition of Terms (Continued)

Symbolic Simulation	Simulation in which some or all inputs are symbolic variables, and functions of these variables are propagated through a design.
System	<p>Any thing consisting of multiple parts that performs a function or set of functions. The boundaries of a system usually follow the structural implementation, but may also cross physical boundaries. For instance, “The memory system xyz shares boards p,q,r,s with other systems.” Systems are typically hierarchical in that a system is often composed of multiple sub-systems.</p> <p>To avoid ambiguity on the term “system,” it is recommended that the appropriate qualifier be stated before its use, such as “CPU memory system,” “radar system,” “DSP system,” etc.</p> <p>Most systems are a component of a larger system. The terms “system” and “component” can therefore be used to refer to the same item, but from different viewpoints: the former when speaking of the item and its constituent parts, and the latter when speaking of the item as a constituent of a larger system. [RASSP, SLD DWG]</p>
System Bus	A bus that connects the processor and the high-speed peripheral functions such as a memory controller, an off chip bus, etc. (See Local Bus). [Member, OCB DWG]
System Chip	A term used to describe highly integrated devices. It is also known as system-on-silicon, system-on-a-chip, system-LSI, system-ASIC, and as a System-Level Integration (SLI) device. [Member, General]
System-on-Chip (SoC)	A single piece of silicon containing multiple virtual components (VCs) to perform a certain defined function.
Target	A VC that receives request packets and sends response packets. It is the agent that responds (with a positive acknowledgment by asserting) to a bus transaction initiated by a initiator, for example, memory.
Target Initial Latency	The number of clocks that the target takes to assert ready for the first data transfer.
Target Subsequent Latency	The number of clocks that the target takes to assert ready from the end of the previous data phase of a burst.
Target-Abort	A termination mechanism that allows a target to terminate a transaction in which a fatal error has occurred, or to which the target will never be able to respond.
Termination	A transaction termination that brings bus transactions to an orderly and systematic conclusion.
Test Bench	A model or collection of models and data files that applies stimuli to a module under test (MUT), compares the response of the MUT with an expected response, and reports any differences observed during simulation. [RASSP, General]
Test Coverage	Test coverage is needed because it has the ability to convey completeness. If a device is defined as bad for any reason (form, fit, or function), the test coverage is by definition less than complete or 100%. (Form and fit will be covered at a later time). Function has two parts. Both are defined as compliance with specifications and behavioral descriptions. Quality refers to how it complies now, and reliability refers to whether it will continue to comply over time. [VSI Alliance, TST 1 1.0]
Testbench	The overall system for applying stimulus to a design and monitoring the design for correct responses.

Table 10: Definition of Terms (Continued)

Theorem Proving	A formal verification technique in which a specification is expressed in a formal logic and proof strategies are utilized to construct a proof that a design obeys the specification.
Timing Analysis Model	Defines the static timing characteristics of the VC.
Timing arc	The input pin to output pin delay between the pins of a VC or cell.
Toggle Coverage	Shows which bits of the signals in the design have toggled.
Transaction	An address phase plus one or more data phases.
Transaction Layer	Refers to point-to-point transfers between blocks or virtual components. It does not define signal names or clock-cycle protocols. Note: Also refers to “Layer” concept. [Member, OCB DWG]
Transition window	The temporal interval containing every instant within a clock cycle at which a specified signal transition may occur.
Transactions	A transaction is a non-atomic transport object which consists of a set of messages or packet chains across ports and along channels.
Transfer State	Any bus clock, during a data phase, in which data is transferred.
Triggering Coverage	Shows whether each process has been uniquely triggered by each of the signals in its sensitivity list.
Turnaround Cycle	A bus cycle used to prevent contention when one agent stops driving a signal and another agent begins driving it. A turnaround cycle must last one clock and is required on all signals that may be driven by more than one agent.
Validation	A “post-silicon” process which proves (with evidence) that a design is valid - physical characterization. For test purposes, the validation process is the use of special purpose test hardware to prove that the product meets the design intent (as opposed to other use of the same equipment as a manufacturing screen). [VSI Alliance, TST 1 1.0]
VC Integration	A process by which a designer combines or reuses multiple VCs to create a large IC. Also termed Block Integration. [VSI Alliance, VSIA]
VC Port	The pad or point of interconnection between the VC and the system chip.
VC Provider	Refers to a person or an entity that originates and sources the VC in the VC transfer process (also known as VC creator). [VCT 1 2.0]
VC User	Entity (also known as VC Integrator) that receives a VC in the Transfer process, as the counter-part to the VC provider. [VCT 1 2.0]
VC Verification	Process of verifying the functionality of a virtual component, i.e., unit test of that component.
VC wrapper	Logic between an existing VC and the VCI.
VCI operation	A transport object consisting of a pair of packets that are transferred in different directions, for example, a single request-response packet pair.

Table 10: Definition of Terms (Continued)

Verification	A “pre-silicon” process normally used during the design phase for gaining confidence that the design will produce the expected (pre-defined) result. An output of verification may be translated into ATE vectors. [VSI Alliance, TST 1 1.0]
Verification Metrics	Techniques for measuring the effectiveness of verification procedures on a design. Broadly divided into hardware code coverage and functional coverage metrics.
Verification Test Suite Migration	A means for translating a test suite that operated on one design level (for example, gate netlist) to another level such as RTL.
Virtual Component (VC)	A block that meets the VSIA specification and is used as a component in the virtual socket design environment. Virtual Components can be of the forms: soft, firm, or hard. A pre-implemented, reusable module of intellectual property that can be quickly inserted and verified to create a single-chip system. VCs are also called megacells or cores.
Virtual Component Interface (VCI)	The VCI is the interface of a Virtual Component. It encompasses all the interface abstraction layers from the most abstract layer down to the lowest specified level. Note that the VSI OCB DWG uses this term internally in their document [11] to refer to their specific interface definitions. The general definition given here encompasses the OCB definition-that is, the OCB VCI is an instance of a VCI.
Virtual Prototype	A computer simulation model of a final product, component, or system. Unlike the other modeling terms that distinguish models based on their characteristics, the term virtual-prototype does not refer to any particular model characteristic. Rather, it refers to the role of the model within a design process; specifically for exploring design alternatives, demonstrating design concepts, and testing for requirement satisfaction/correctness. See prototype, physical-prototype. [RASSP, SLD DWG]
Virtual Prototyping	The activity of configuring (constructing) and using (simulating) a computer software-based model of a product, system, or component to explore, test, demonstrate, and/or validate the design, its concept, and/or design features, alternatives, or choices. Specifically, it is the act of using the virtual-prototype model as if it were an example of the final (physical) product. See prototype, virtual prototype. [RASSP, SLD DWG]
Virtual Socket Interface	A set of proposed specifications needed to enable system-level integration on a chip using VCs resulting in rapid development of product. This enables IC design using a component-based paradigm. [VSI Alliance, VSIA]
Visited State Coverage	Shows how many states of a Finite State Machine were entered during simulation.
Wait	A bus clock in which no transfer occurs.

C. Glossary of Acronyms

A/D; ADC	Analog to Digital Converter
AC	Alternating current
ADC	Analog-to-digital converter
AGF	Annotated GDSII format
ALF	OVI Advanced Library Format, http://www.eda.org/alf/
AMS	Analog Mixed Signal
API	Application program interface
ASIC	Application-specific integrated circuit
ATPG	Automatic Test Pattern Generation
AVCI	Advanced Virtual Component Interface (VCI)
BAP	Bias Access Point
BFM	Bus Functional Model
BiCMOS	Bi-Polar Complementary Metal Oxide Silicon
BIST	Built-in Self Test
BNF	An acronym for “Backus Normal Form” (sometimes called, “Backus-Naur Form”) used to describe syntax in computer languages.
bps	bits per second
BVCI	Basic Virtual Component Interface (VCI)
CAD	Computer Aided Design
CAN	Controller Area Network
CMOS	Complementary Metal Oxide Silicon
CP	Charge Pump
CSP	Control signal processor
D/A; DAC	Digital to Analog Converter
DC	Direct current
DEF	Design Exchange Format. This is a format from Cadence Design Systems. It is used for a description of physical design information. This includes the netlist and circuit layout.
DFM	Design for Manufacturing (DFM) - refers to specific activities during the design process, which ensure the design is optimized for the fabrication process that will create the product. This is described in the Design Rules, checked by DRCs, and verified by product yield. [Member, TST 1 1.0]

DFT	Design for Test (DFT) - refers to specific activities during the design process, which provide the ability to control and observe on silicon needed by test to determine the quality of the product. These activities should be described by guidelines, checked by simulation, and verified by the cost of test. [Member, TST 1 1.0]
DMA	Direct Memory Access
DNL	Differential Non-linearity
DRC	Design Rule Check
DSM	Deep Submicron
DSP	Digital Signal Processor
DVD	Digital Versatile Disk
DWG	Development Working Group
ECL	Emitter Coupled Logic
EM	Electro Magnetic
EPI	Epitaxial substrate layer
ESPF	Extended Standard Parasitic Format
FIFO	first-in, first-out
FSM	Finite State Machine
Gbps	Gigabits per second
GCF	General Constraint Format
GDSII	Graphical Design System
GHz	Giga-Hertz
GIF	Geometric Image Format
GSM	Global system for mobile communications
HDL	Hardware Design Language
HDS	Hardware-dependent Software
I/O	Input/Output
ICE	In-Circuit Emulator
IDDQ; IDDq	IDD Quiescent Current - This is a measurement of power supply current with the device in a static state. IDDq tests are used to increase fault coverage, improve reliability, and to screen devices for battery- or low-power applications.
IEEE	Institute of Electrical and Electronic Engineers
INL	Integral Non-linearity
IP	Intellectual Property
IP(P)	Intellectual Property (Protection)
ISA	Instruction Set Architecture
ISV	Independent Software Vendor
ITL	Interpolated Table Lookup-format

ITRS	International Technology Roadmap for Semiconductors,
ITU	International Telecommunication Union
LBIST	Logic Built In Self-Test
LEF	Layout Exchange Format
LNA	Low-noise amplifier
LPE	Layout Parasitic Extraction
LSB	Least Significant Bit. This is used for binary representation of integers on the digital side of ADC and DAC. One LSB is the resolution, and is equal to the analog range divided by 2 to the power of N (number of bits in the digital range).
LVS	Layout Versus Schematic
MAST	Analog Hardware Description Language, owned by Analogly. This is not an acronym.
Mbps	Megabytes per second
MCF	Miller Coupling Factor
MIPS	Million instructions per second
MPSOC	multi-processor system-on-chip
MSB	Most Significant Bit. This is used for binary representation of integers on the digital side of ADC and DAC. The MSB switches at the midpoint of the analog range.
MTF	Mean-time-to-failure
NLDM	Non-Linear Delay Model
NMI	Non-maskable interrupt.
OCB	On-chip Bus
OLA	Open Library API, http://www.si2.org/OLA/olaoverview.htm
OMF	Open Model Forum
OTA	Operational Transconductance Amplifier
OTH	Over-the-hierarchy
OVI	Open Verilog International, now called Accellera,
PCI	Peripheral Component Interconnect, the industry-standard PCI bus.
PDEF	Physical Design Exchange Format
PIN	Peripheral interconnect model
PLI	Procedural Language Interface
PLL	Phase Locked Loop
POST	Power-on self-test. A series of diagnostic routines performed when a system is powered up.
PVCI	Peripheral Virtual Component Interface (VCI)
PWL	Piece-wise linear
QTY	VP quality

RAM	Random Access Memory
RF	Radio Frequency
RMS	Root mean square
RTL	Register Transfer Logic
RTOS	Real-Time Operating System
SAP	Substrate access port
SDF	Standard Delay Format
SI	Signal integrity
SLI	System Level Integration
SLM	System Level Macro
SoC	System-on-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
Sps	Samples per second
SR	Shift Register
STIL	Standard Test Interface Language
TAP	Test Access Port
Theta J-A	Package Heat dissipation characteristic
TLF	Timing Library Format
TTM	Time-To-Market
UART	Universal Asynchronous Receiver Transmitter
UDSM	Ultra-deep sub-micron
uP	Micro Processor
URL	Uniform Resource Locator
VC	Virtual Component
VCD	Verilog Change Dump
VCI	Virtual Component Interface, an OCB-standard for communicating between a bus and a virtual component, which is independent of any specific bus or VC protocol.
VC-LEF	Virtual component library exchange format
VCO	Voltage Controlled Oscillator
VERILOG	Verilog Hardware Description Language
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuits
VSI	Virtual Socket Interface
VSIA	VSI Alliance
Vt	Voltage Threshold
WGL	Waveform Generation Language

D. Compliance Policy

Many companies wish to establish and publicize that their products are “VSIA compliant.” The following policy and procedure describes how to determine VSIA compliance and provides an easy-to-use format for publicizing compliance.

It can be complex to determine and show VSIA compliance, since there are many recommended formats and documents in the VSIA specifications and a wide range of requirements to cover. However, not all compliance requirements apply to all products, and users of a product will differ in their concern for each compliance issue. Furthermore, as VSIA specifications are revised and new ones are added, the list of deliverables required for full and current compliance must change. The following policy takes these complexities into consideration, and resolves them

Those using VSIA compliance information need to study the VSIA specifications to understand the full meaning of the data.

Notice of Copyrights and Trademarks

Use of the following procedure requires reproduction and use of Table 1 of this document (herein referred to as “table”), the VSIA Deliverables Summary, which is copyrighted by the VSIA, and reproduction and use of the VSIA Compliance Trademark. These items may be reproduced and used only for claiming and showing specific compliance of products with VSIA specifications, and if the user abides by the following terms specified for VSIA compliance. Any company (VSIA member or non-member) that abides by these terms may use the Trademark and table free of charge.

Compliance Claim

A claim of VSIA compliance must be made in reference to a specific version of the table, which is maintained by the VSIA. The table includes two columns entitled “Comply?” and “Comments.” The company completes the table by including check marks as applicable in the “Comply?” column and short comments or references to subsequent notes, in the “Comments” column.

A compliance claim is made by the use of the specified version of the Trademark. The Trademark includes the version designation within it, which must be the same version as that of the table used.

VSIA Revisions

When a VSIA specification is revised or a new one is released, the VSIA revises the Deliverables Document. The table and Trademark are revised at the same time to include the same version designation as the new Deliverables Document.

Form of VSI Alliance Trademark

The form of the Trademark is:

VSIA [Ver] Compliant[™]

[Ver] is the version designation and is in the form of a single-decimal number (such as 1.0, 2.0, etc.). If the version of the Deliverables Document is 2.0, the Trademark will appear as:

VSIA 2.0 Compliant[™]

The style of the font must be Arial (or equivalent), bold, with underline.

Use of the Trademark and Table and Determining Compliance

A company may claim VSIA compliance for a specific product by using the Trademark, provided that the company completes a compliance report (by hand or via the web-based VSIA Compliance System at www.vsi.org) that meets the following six terms:

1. Compliance Report

- a) A “Compliance Report” must promptly be provided to any requestor. The company should download and complete the Web resident table (www.vsi.org) in its entirety and include it in its Compliance Reports.

- b) The Compliance Report is a document created by the company that must include a completed table. A “Comments Section” immediately after the table for notes concerning the marked items in the table is optional.
 - c) ALL of the relevant mandatory items must be accurately marked with a “yes,” “no” or “NA” (NA meaning not applicable) in the “Comply?” column of the table.
 - d) Those items that do not apply to the product should be marked “NA” in the “Comply?” column of the table.
 - e) Relevant but non-mandatory items may also be check marked at the company's option in the “Comply?” column of the table.
 - f) The company, at its option, may fill in the “Comments” section of the Compliance Report, describing how each required deliverable was verified to be compliant. The “Comments” column explanation may be expanded by reference to the subsequent “Comments” section.
 - g) A company using the Trademark and table may, at its option upgrade to new versions when the VSIA revises the Deliverables Document. It is recommended that a new product claim of compliance comply with the latest version of the deliverables table.
2. Compliance pertains to individual products, not to companies. A company must supply a separate Compliance Report for each product (tool or VC) for which it claims VSIA compliance. Any report must be published or furnished promptly on request.
 3. The entire table must be provided in the Compliance Report, not excerpts. The table is copyrighted and permission to reproduce it is subject to the condition that it may be reproduced only in whole. The VSIA copyright notice should also be included with the table. Product information that includes only partial compliance information or a compliance summary should include directions for obtaining the full table.
 4. A company may provide more than one compliance report for a particular product. This enables the company to provide more optional information to some requestors than to others. However, each report must satisfy the VSIA requirements.
 5. If an item or section is marked “NA” (not applicable), it means that the item does not apply to this particular-type of VC (e.g., the Analog Mixed Signal items would not apply to a digital VC, or the On Chip Bus items would not apply to an Analog Mixed Signal VC). “NA” may NOT be used when the item is applicable to the product, but the company cannot or does not want to supply it.
 6. If an item is checked in the “Comply?” column, it also means that the company will provide this item in the Virtual Component data transfer package.

Any company that meets all of the six requirements listed above may use the Trademark in its product literature for the product that meets the above requirements.

Verification

Compliance may be self-verified, by the use of tools, test cases, or services. This procedure allows universities or independent test companies to play a role in VSIA compliance, responding to industry demands.